CLAIMS

1. (Canceled)

2. (Canceled)

3. (currently amended) ~~The~~ A method ~~as claimed in claim 2~~ of segmenting variable-size packets, each packet being associated with one of a plurality of defined data streams, the method comprising steps of:

concatenating packets of each data stream, from among said plurality of data streams, into concatenated packets; and

dividing each of said concatenated packets into equal-size segments,

wherein said steps of concatenating and dividing are constrained by an adaptive delay threshold;

and wherein the adaptive-delay threshold is determined by an allocated transfer rate to said each data stream;

and wherein the adaptive delay threshold is governed by a transfer rate controller.

4. (currently amended) The method as claimed in claim ~~2~~ 3 wherein the ~~magnitude of~~ the adaptive delay threshold is data-stream dependent.

5. (canceled)

6. (canceled)

7. (currently amended) In a network comprising source nodes and sink nodes, the method as claimed in claim ~~1~~ 3 wherein said ~~concatenation~~ step of concatenating is applied at the ingress port of a source node.

8. (currently amended) In a network comprising source nodes and sink nodes, the method as claimed in claim ~~1~~ 3 wherein said ~~concatenation~~ step of concatenating is applied at the output port of a source node.

9. (canceled)

10. (currently amended) In a switching node receiving packets from a plurality of incoming channels, a method of two-phase packet segmentation ~~wherein the first phase segments individual packets and the second phase segments an aggregate of packets~~ comprising:

segmenting individual packets in a first phase into first-phase segments using a plurality of first-phase segmentation circuits;

segmenting an aggregate of packets in a second phase into second-phase segments using a plurality of second-phase segmentation circuits;

switching an output of said first-phase segmentation circuits to said second-phase segmentation circuits under control of a routing algorithm;

wherein said routing algorithm selects routes from an incoming channel to a sink node using a method of maximum aggregation probability.

11. (canceled)

12. (canceled)

13. (currently amended) The method as claimed in claim 10 wherein said first-phase segments are of equal size and said second-phase segments are of equal size and the size of a second-phase segment is an integer multiple of the size of a first-phase segment.

14. (canceled)

15. (canceled)

16. (canceled)

17. (canceled)

18. (canceled)

19. (currently amended) The method as claimed in claim ~~18~~ 10 wherein a first-phase segmentation circuit is allocated to an incoming channel.

20. (canceled)

21. (canceled)

22. (original) A data structure to enable merging equal-size null-padded data segments into new equal-size data segments having reduced null-padding, the data segments belonging to $K > 1$ data streams, the data structure comprising:

(i) An array "A" of fractional segments having K entries, each entry dedicated to a data stream;

(ii) An array "B" of complete segments having K1 > K entries; and

(iii) a control matrix "C" having K records, each record dedicated to a data stream and having four fields to indicate, for a corresponding stream, the stream's delay threshold, the stream's current delay, the fill of a respective fractional-segment in array "A", and the address of a complete segment in array "B".

23. (original) The data structure as claimed in claim 22 wherein the size of each of said new equal-size data segments is an integer-multiple of the size of each of said equal-size null-padded data segments.

24. (original) The data structure as claimed in claim 22 wherein array "A" is directly indexed by a stream identifier.

25. (original) The data structure as claimed in claim 22 wherein array "A" is replaced by a pointer array and a segment-storage array.

26. (original) In conjunction with the data structure as claimed in claim 22, a method for data segmentation including steps of

(a) Receiving a plain segment of a stream k, $0 \leq k < K$;

(b) Merging said plain segment with data content of array "A" at storage position k;

(c) Appending a complete segment resulting from said merging to a queue associated with data stream k in array "B"; and

(d) Overwriting a fractional segment resulting from said merging in memory "A" at position k.

27. (original) In conjunction with the data structure as claimed in claim 22, a method of controlling data segments transfer, the method including steps of:

(e) Receiving from a transfer rate controller a prompt to transfer a data segment of a stream k, $0 \leq k < K$;

(f) Transferring a complete segment belonging to data stream k in array "B" if said complete segment exists; else

(g) Transferring a fractional segment belonging to data stream k in array "A" if said fractional segment exists and has already been prompted by said rate controller a predefined number of times; else

(h) Return a no-action indication to rate controller.

28. (original) The method as claimed in claim 26 wherein a plurality of plain segments are processed concurrently.

29. (original) The method as claimed in claim 26 wherein pointers to transferred segments are placed in a transfer queue.

30. (original) A compact-segmentation apparatus operable to segment variable-size packets into compact fixed-size segments, the apparatus comprising

(a) a packet segmentation circuit;
(b) an enqueueing controller;
(c) a principal data memory;
(d) an auxiliary data memory;
(e) a control memory;
(f) a dequeueing controller; and
(g) a transfer-rate controller;

wherein

said packet segmentation circuit receives variable-size packets and segments each of said variable-size packets into plain segments,

said packet segmentation circuit identifies a data stream associated with each one of said variable-size packets,

said enqueueing controller communicates with said control memory, said principal data memory, and said auxiliary data memory, and concatenates said plain segments of a data stream with previously-received segments of same data stream,

said transfer-rate controller selects a selected data stream, and

said dequeueing controller selects data segments, belonging to said selected data stream, from waiting data segments in said principal data memory and said auxiliary data memory for transfer downstream.

31. (currently amended) The ~~compact packet segmentation circuit~~ apparatus as claimed in claim 30 wherein the rate controller is driven by a service-quality controller.

32. (currently amended) The ~~compact packet segmentation circuit~~ apparatus as claimed in claim 31 wherein the service-quality controller is source-node driven.

33. (currently amended) The ~~compact packet segmentation circuit~~ apparatus as claimed in claim 31 wherein the service-quality controller is driven by a source node controller.

34. (currently amended) The ~~compact packet segmentation circuit~~ apparatus as claimed in claim 30 wherein the principal data memory is structured as a multi-head interleaved linked list.

35. (original) The apparatus as claimed in claim 31 wherein a segment is ready for transfer by the dequeueing controller if it is a complete segment waiting in the principal data memory or a fractional segment waiting in the auxiliary data memory and has already been prompted by the rate controller a predefined number of times.

36. (original) A circuit for fast concatenation of a first packet of a known length and a second packet of a known length into a complete segment of a predefined length, the circuit comprising a shift connector, a memory array, and a register array, the length of said first packet being smaller than said predefined length and the length of said second packet being less than said predefined length, wherein

said first packet is copied onto said register array, said shift connector performs a concatenation process that concatenates said second packet with said first packet onto said register array placing any remainder resulting from said concatenation process in said memory array.

37. (original) The circuit as claimed in claim 36 wherein the shift connector is constructed from arrays of shift connectors of a smaller size.

38. (original) The circuit as claimed in claim 37 wherein each array comprises identical shift connectors and the sizes of shift connectors in different arrays are different.

39. (canceled)

40. (canceled)

41. (canceled)

42. (canceled)